Listing of claims:

1. (Currently Amended) An apparatus for controlling an output current (I_{OUT}) that is delivered to a load circuit by a power device, the apparatus comprising:

a current sense circuit that is arranged to provide a sense signal that is responsive to the output current, wherein the current sense circuit is coupled to the load circuit such that the operating current of the apparatus does not dramatically rise when a short-circuit condition is present across the load circuit, wherein the current sense circuit comprises a first transistor that is series coupled to the load circuit via a resistor such that the sense signal corresponds to a voltage associated with the resistor, wherein the first transistor includes a control terminal that is biased in common with the power device;

a first transistor circuit that is arranged to deactivate the power device when a short-circuit detection signal is asserted;

a second transistor circuit that is arranged to couple a small current to the load circuit when the short-circuit detection signal is asserted such that the apparatus automatically returns to a normal operating mode when the short-circuit condition is removed from the load circuit, wherein the small current corresponds to a nominal level such that the energy loss is minimized during the short-circuit condition; and

a differential comparator circuit that includes: a first input that is coupled to the load circuit, a second input that is coupled to the sense signal, and an output that is associated with the short circuit detection signal, wherein the comparator circuit is arranged to assert the short-circuit detection signal as a logic level when the sense signal indicates that the short-circuit condition is detected across the load circuit.

2. (Cancelled)

3. (Original) The apparatus of Claim 1, wherein the first transistor circuit comprises a p-type transistor that includes a source terminal that is coupled to a power supply node, a gate terminal that is arranged to receive the short-circuit detection signal, and a drain terminal that is

coupled to a control terminal of the power device such that the power device is deactivated when the short-circuit detection signal is asserted as an active low signal.

4. (Currently Amended) ~~The apparatus of Claim 1,~~ An apparatus for controlling an output current (I_{OUT}) that is delivered to a load circuit by a power device, the apparatus comprising:

a current sense circuit that is arranged to provide a sense signal that is responsive to the output current, wherein the current sense circuit is coupled to the load circuit such that the operating current of the apparatus does not dramatically rise when a short-circuit condition is present across the load circuit, wherein the current sense circuit comprises a first p-type transistor that includes a source terminal that is coupled to a power supply node, a gate that is coupled to a control node, and a drain that is coupled to the load circuit through a resistor such that the sense signal corresponds to a voltage that is associated with the resistor; and wherein the first transistor circuit comprises a second p-type transistor that includes a source terminal that is coupled to the power supply node, a gate terminal that is arranged to receive the short-circuit detection signal, and a drain terminal that is coupled to a control terminal of the power device at the control node such that the power device and the first-p-type transistor are deactivated when the short-circuit detection signal is asserted as an active low signal;

a first transistor circuit that is arranged to deactivate the power device when a short-circuit detection signal is asserted;

a second transistor circuit that is arranged to couple a small current to the load circuit when the short-circuit detection signal is asserted such that the apparatus automatically returns to a normal operating mode when the short-circuit condition is removed from the load circuit, wherein the small current corresponds to a nominal level such that the energy loss is minimized during the short-circuit condition; and

a differential comparator circuit that includes: a first input that is coupled to the load circuit, a second input that is coupled to the sense signal, and an output that is associated with the short circuit detection signal, wherein the comparator circuit is arranged to assert the short-circuit detection signal as a logic level when the sense signal indicates that the short-circuit condition is detected across the load circuit.

5. (Original) The apparatus of Claim 1, wherein the second transistor circuit comprises a first p-type transistor that includes a source terminal that is coupled to a power supply node, a gate terminal that is arranged to receive the short-circuit detection signal, and a drain terminal that is coupled to a local power supply node; and a second p-type transistor that includes a source terminal that is coupled to the local power supply node, a gate terminal that is arranged to receive a bias signal, and a drain terminal that is coupled to the load circuit, wherein the first p-type transistor is arranged to couple the power supply node to the local supply node when the short-circuit detection signal is asserted as an active low signal such that the second p-type transistor is operates as a current source to provide the small current when the short-circuit detection signal is asserted.

6. (Original) The apparatus of Claim 5, the second transistor circuit further comprising a third p-type transistor that is arranged to provide the bias signal in response to a reference current.

7. (Currently Amended) ~~The apparatus of Claim 1, further comprising~~ An apparatus for controlling an output current (I_{OUT}) that is delivered to a load circuit by a power device, the apparatus comprising:

a current sense circuit that is arranged to provide a sense signal that is responsive to the output current, wherein the current sense circuit is coupled to the load circuit such that the operating current of the apparatus does not dramatically rise when a short-circuit condition is present across the load circuit;

a first transistor circuit that is arranged to deactivate the power device when a short-circuit detection signal is asserted;

a second transistor circuit that is arranged to couple a small current to the load circuit when the short-circuit detection signal is asserted such that the apparatus automatically returns to a normal operating mode when the short-circuit condition is removed from the load

circuit, wherein the small current corresponds to a nominal level such that the energy loss is minimized during the short-circuit condition;

a differential comparator circuit that includes: a first input that is coupled to the load circuit, a second input that is coupled to the sense signal, and an output that is associated with the short circuit detection signal, wherein the comparator circuit is arranged to assert the short-circuit detection signal as a logic level when the sense signal indicates that the short-circuit condition is detected across the load circuit; and

a level shifter circuit that is responsive to the sense signal, wherein the level shifter circuit is arranged to provide another sense signal that is related to the sense signal by a level shift, wherein the sense signal is coupled to the second input of the comparator circuit as the another sense signal.

8. (Original) The apparatus of Claim 7, wherein the level shifter circuit is arranged to provide a predetermined voltage level to the second input of the comparator circuit after the short circuit detection signal is asserted, wherein the predetermined voltage level is different from a power supply potential to provide a minimum over-drive to the comparator circuit while the load circuit is short-circuited.

9. (Original) The apparatus of Claim 7, wherein the level shifter circuit comprises: a first n-type transistor that includes a drain that is couple to the short-circuit detection signal, a gate that is arranged to receive the sense signal, and a source that is coupled to the second input of the comparator circuit at a first node; a second n-type transistor that includes a drain that is coupled to the first node, a gate that is arranged to receive a bias signal from a second node, and a source that is coupled to a power supply node; and a third transistor that is includes a gate and drain that are coupled to the second node, and a source that is coupled to the first node.

10. (Original) The apparatus of claim 9, wherein the third n-type transistor is ratio sized with respect to the second n-type transistor such that the third transistor is arranged to provide the minimum over-drive to the comparator circuit while the load circuit is short-circuited.

11. (Original) The apparatus of claim 9, the level shifter circuit further comprising a fourth n-type transistor that includes a gate and drain that are coupled to the second node, and a source that is coupled to the power supply node, wherein the fourth n-type transistor is ratio sized to the second n-type transistor to provide the biasing signal in response to a reference current that is applied to the second node.

12. (Original) The apparatus of claim 1, wherein the comparator circuit includes at least one inverting gain stage.

13. (Currently Amended) An apparatus for controlling an output current (I_{OUT}) that is delivered to a load circuit by a power device, the apparatus comprising:

a current sense means, wherein the current sense means is arranged to provide a sense signal that is responsive to the output current, wherein the current sense means is coupled to the load circuit such that there is approximately no DC current in the apparatus when a short-circuit condition is present across the load circuit, wherein the current sense means comprises a transistor means that is series coupled to the load circuit via a resistor means such that the sense signal corresponds to a voltage associated with the resistor means, wherein the transistor means is arranged for common biasing with the power device;

a disabling means that is arranged to disabled the power device when a short-circuit detection signal is asserted;

a recovery current means that is arranged to provide a small current (I) to the load circuit when the short-circuit detection signal is asserted such that the apparatus automatically returns to a normal operating mode when the short-circuit condition is removed from the load circuit;

a differential comparator means that is arranged to assert the short-circuit detection signal as a logic level when the sense signal indicates that the short-circuit condition is detected across the load circuit; and

a minimum over-drive means that is arranged to maintain at least one input signal to the comparator means at a minimum over-drive level (Vmin_OD) when the short circuit condition is present.

14. (Currently Amended) The apparatus of Claim 13, wherein ~~the current sense means includes a~~ the transistor means ~~that~~ is sized relative to the power device according to a size ratio (m) such that the short circuit current limit is determined by the size ratio (m).

15. (Currently Amended) The apparatus of Claim 14, wherein the ~~current sense means further comprises a~~ resistor means ~~that~~ has a value corresponding to R, wherein the short circuit current limit (Isc) is determined as: Isc = m*Vgs/R, wherein Vgs corresponds to a gate-source voltage of a transistor, which is related to a threshold voltage and associated with the transistor means, and wherein the threshold voltage is dependent on temperature.

16. (Original) The apparatus of Claim 13, wherein the recovery current means includes a current source means that is selectively activated when the short-circuit detection signal is asserted to provide the small current (I) over a recovery time (t), wherein the recovery time (t) is determined as: t = CL*Vmin_OD/(I – Vmin_OD/RL), where Vmin_OD is a minimum overdrive voltage, CL is a capacitor associated with the load circuit, RL is a resistance associated with the load circuit.

17. (Currently Amended) A method for providing a current (I_{OUT}) to a load circuit from a power device, the method comprising:

biasing a transistor circuit in common with the power device;

coupling a current from the transistor circuit to the load circuit through a resistor circuit;

sensing a the current though the resistor circuit to ~~associated with the power device~~ to provide a sense signal that is responsive to the output current from the power device;

sensing an output voltage that is associated with the load circuit;

differentially comparing the sense signal to the sensed output voltage ~~differentially~~;

asserting a logic level short-circuit detection signal when the sensed output voltage is less than the sense signal;

disabling the power device when the short-circuit detection signal is asserted;

enabling a current source when the short-circuit detection signal is asserted, wherein the current source is coupled to the load circuit;

increasing the output voltage across the load with the current source when the short-circuit condition is removed from the load circuit;

detecting when the short circuit condition is removed from the load circuit; and

enabling the power device when the short-circuit condition is detected as removed from the load circuit.

18. (Currently Amended) The method of claim 17, further comprising: changing ~~a~~ the sense signal in response to an operating temperature associated with the power device such that a threshold associated with the detection of the short-circuit condition is adjustable.

19. (Original) The method of Claim 17, further comprising: maintaining a minimum overdrive condition such that the output voltage must increase above a predetermined amount after the short circuit condition is detected as removed from the load circuit.

20. (Original) The method of claim 17, further comprising: disabling the current source when the short-circuit condition is detected as removed from the load circuit.

21. (New) The apparatus of Claim 4, further comprising: a level shifter circuit that is responsive to the sense signal, wherein the level shifter circuit is arranged to provide another sense signal that is related to the sense signal by a level shift, wherein the sense signal is coupled to the second input of the comparator circuit as the another sense signal.

22. (New) The apparatus of Claim 21, wherein the level shifter circuit is arranged to provide a predetermined voltage level to the second input of the comparator circuit after the short circuit detection signal is asserted, wherein the predetermined voltage level is different from a power supply potential to provide a minimum over-drive to the comparator circuit while the load circuit is short-circuited.

23. (New) The apparatus of Claim 4, wherein the second transistor circuit comprises a first p-type transistor that includes a source terminal that is coupled to a power supply node, a gate terminal that is arranged to receive the short-circuit detection signal, and a drain terminal that is coupled to a local power supply node; and a second p-type transistor that includes a source terminal that is coupled to the local power supply node, a gate terminal that is arranged to receive a bias signal, and a drain terminal that is coupled to the load circuit, wherein the first p-type transistor is arranged to couple the power supply node to the local supply node when the short-circuit detection signal is asserted as an active low signal such that the second p-type transistor is operates as a current source to provide the small current when the short-circuit detection signal is asserted.

24. (New) The apparatus of Claim 7, wherein the current sense circuit comprises a first transistor that is series coupled to the load circuit via a resistor such that the sense signal corresponds to a voltage that is associated with the resistor, wherein the first transistor includes a control terminal that is biased in common with the power device.

25. (New) An apparatus for controlling an output current (I_{OUT}) that is delivered to a load circuit by a power device, the apparatus comprising:

a current sense means, wherein the current sense means is arranged to provide a sense signal that is responsive to the output current, wherein the current sense means is coupled to the load circuit such that there is approximately no DC current in the apparatus when a short-circuit condition is present across the load circuit;

a disabling means that is arranged to disabled the power device when a short-circuit detection signal is asserted;

a recovery current means that is arranged to provide a small current (I) to the load circuit when the short-circuit detection signal is asserted such that the apparatus automatically returns to a normal operating mode when the short-circuit condition is removed from the load circuit;

a level shifting means that is responsive to the sense signal, wherein the level shifting means is arranged to provide a level shifted sense signal that is related to the sense signal by a level shift;

a differential comparator means that is arranged to assert the short-circuit detection signal as a logic level when the level shifted sense signal indicates that the short-circuit condition is detected across the load circuit; and

a minimum over-drive means that is arranged to maintain at least one input signal to the comparator means at a minimum over-drive level (Vmin_OD) when the short circuit condition is present.

26. (New) A method for providing a current (I_{OUT}) to a load circuit from a power device, the method comprising:

sensing the current though a resistor circuit to provide a sense signal that is responsive to the output current from the power device;

sensing an output voltage that is associated with the load circuit;

differentially comparing the sense signal to the sensed output voltage;

level shifting the sense signal to provide a level shifted sense signal that is related to the sense signal by a level shift;

asserting a logic level short-circuit detection signal when the sensed output voltage is less than the level shifted sense signal;

disabling the power device when the short-circuit detection signal is asserted;

enabling a current source when the short-circuit detection signal is asserted, wherein the current source is coupled to the load circuit;

increasing the output voltage across the load with the current source when the short-circuit condition is removed from the load circuit;

detecting when the short circuit condition is removed from the load circuit; and

enabling the power device when the short-circuit condition is detected as removed from the load circuit.